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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,218	11/20/2003	Wen-Chou Vincent Wang	ALTRP100/A1198	3208

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BEYER WEAVER & THOMAS, LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/719,218	WANG ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 37-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16,37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on December 19, 2005 has been entered and forwarded to the Examiner on December29, 2005.

Therefore claims 2,5 and 6 as amended by the amendment and claims 1,3-4, 7-16 as previously recited and presently newly added claims 37-40 are currently pending in the Application.

Claims 17 to 36 have been cancelled.

Election/Restrictions

Applicant's election without traverse of claims 1-16 (Gr. I) in the reply filed on Dec. / 19/2005 is acknowledged.

Information Disclosure Statement

To date no IDS has been filed in this Application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 to 16, 37-40 are rejected under 35 U.S.C. 102(b) as being unpatentable over Distefano . (U.S. Patent No. 6,127,724, herein after Distefano).

With respect to claim 1 Distefano describes a semiconductor package comprising a die having a plurality of layers of low-K dielectric material, (Distefano figure 7 # 432-diefigure 1 # 32 die dielectric layers 20,26) the die having a top surface, a bottom surface, and a plurality of side surfaces, each surface having associated corner and edge regions, (Distefano figures 1and 7, etc.) a wire bonding packaging substrate having a plurality of electrical contacts, (Distefano figure1 # 66, col. 1 line 61, figure 7 # 440) the packaging substrate being positioned under the die (Distefano fig.1 66 under 32, col.8 lines 55-60, figure 7 shaded portion under 432) ; a plurality of interconnects electrically connecting the die to the plurality of electrical contacts, (DIstefano figure 1 54, col. 7 lines figure 7 # leads not numbered similar to flexible leads 54 in figure 3) a molding interface material applied to at least a portion of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die; (Distefano figure 1 52 figure 7, col. 13 lines 55 to 65) and a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material. (Distefano ,figure 1 58 figure 7 # 459).

With respect to claim 2 Disteano describes a semiconductor package as recited in claim 1, wherein the molding interface material is configured to introduce compressive stress to the die, (it is inherent that the same material disclosed by Distefano as that claimed by Applicants' will recite the same compressive stress as claimed herein) thereby strengthening the die against the at least one of tensile and shear stresses. (it is further inherent that increase in

one kind of stress (comrpesssive) will reduce the other (tensile and /or shear stress and strengthen the die against the at least one of tensile and shear stresses.

The recitation, 'wherein the molding interface material controls by applying compressive stress to the die, thereby strengthening the die against the at least ' one of tensile and shear stresses " is taken to be a hybrid functional and product by process recitation for which patentable weight cannot be given.

With respect to claim 3 Distefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is polyimide. (Distefano col. 8 lines 9 to 16) .

With respect to claim 4 Di Stefano describes a semiconductor package aq recited in claim 3, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die. (Di Stefano figure 7 encapsulant 458 on sides of 432).

With respect to claim 5 Di Stefano describes a semiconductor package as recited in claim 4, wherein the molding adjacent portion of the packaging interface material is also on a corresponding substrate in order to secure the die to the packaging substrate. (Distefano figures 1-7).

The limitation " in order to secure " is also taken to be a product by process limitation for which no patentable weight can be given. See discussion above under claim 2 (incorporated here by reference) .

With respect to claim 6 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material covers multiple non-contiguous regions to the top surface of the die. (Distafano figures1- 7) .

With respect to claim 7 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape. (Distafano figures 1- 7)

With respect to claim 8 Di Stefano describes a semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape. (Distafano figures1-7)

With respect to claims 9 Di Stefano describes a semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns. (Claim 9 depends from claim 6 and the product by process limitation not being given patentable weight in claim 6 is also applicable here.).

With respect to claims 10 and 12, 11Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the top surface of the die excluding corner regions. (Distafano figure 7)

With respect to claim 1 1 Di Stefano describes a semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns. (DiStefano figures, entire patent)

With respect to claim 13 Di Stefano describes a semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns. (rejected for same reasons as claim 11)

With respect to claim 14 Di Stefano describes a semiconductor package as recited in claim 1, wherein the molding interface material has a coefficient of thermal expansion between 5 ppm and 40 ppm. (Distefano col. 8 lines 17-40, col. 9 lines 18 to 65).

With respect to claim 15 Di Stefano describes a semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the die such that a stress buffer zone is established between the die and the molding cap. (DiStefano figures 1- 7 , col. 13 lines 53-62).

With respect to claim 16 Di Stefano describes a semiconductor package as recited in claim i , wherein the plurality of layers includes extra low-K dielectric material. (Di Stefano col. 6 line 3 polyimide known in the art to be low k-dielectric material).

With respect to claim 37 DiStefano describes a Semiconductor package as recited in claim I where the molding interface material is a layer positioned between and in contact with the die and the molding cap. (Distefano 52 between 32 and 58 figures)

With respect to claim 38 DiStefano describes a semiconductor package as recited in claim 1 wherein the plurality of low-K dielectric material has a CTE between the range of 20 ppm and 50 ppm. (Distefano col. 8 lines 17-40, col. 9 lines 18 to 65).

With respect to claim 39 Di Stefano describes a semiconductor package as recited in claim 38, wherein the plurality of low-K dielectric material has a dielectric constant between 2.6 and 3.5. (polyimide dielectric constant between 3.1-3.4, and other materials described in DiStefano)

With respect to claim 40 DiStefano describes a semiconductor package as recited in claim 38, wherein the plurality of low- K dielectric material has a dielectric constant between 2.2 and 2.6. (DiStefano col. 7 line 51 to col. 8 line 16).

Response to Arguments

Applicant's arguments filed December 19, 2005 have been fully considered but they are not persuasive for the following reasons :

Applicants' first contention that DiStefano employs no structure that corresponds to the molding interface material is wrong . Distefano describes in its figures 1, 7 etc. # 52- which in col. 7 lines 50 to col. 8 lines 16 includes the same epoxy from same company Dow similar to Applicants' 216 described as any suitable material –page 11 lines 18-22. and DiStefano describes encapsulant 58 (col 7 line 57) which is similar to Applicants' molding cap as defined in their specification page 9 last line and page 10 lines 2-5.

Applicants' next contention that DiStefano does not describe plurality of layers of low-K dielectric material is wrong DiStefano in figure 1 etc describes layers 20, 26 which are low-K dielectric layers.

Applicants' contention that DiStefano"s teachings should be limited to conventional SI die as opposed to Low-K Si die is wrong As per Applicants' specification page 1 lines 12-18 , etc. a low –K Si die is a dice having plurality of layers of low dielectric constant (Low-K) materials.

It is very clear to one of ordinary skill in the art that DiStefano's dielectric layers include " polyimide " the same material recited in Applicants' claim 3 , therefore either Applicants' claim 3 does not include a Low-K dielectric SI die or Applicants' argument is merit less.

It is further noted that one of ordinary skill in the art would know that polyimide has a Low dielectric constant between approx 3.1 and 3.4 and Applicants' have specifically recited this material is claim 3 and further in newly added claim 39 have specified their dielectric material has a dielectric constant between 2.6 and 3.5 and polyimide having dielectric constant between approx 3.1 and 3.4 falls within the recited range 2.6 to 3.5.

Therefore DiStefano describes a Low-K SI die and not a conventional chip or die only.

DiStefano also describes plurality of layers of low_ K dielectric material (at least layer s 20, 26 etc.) .

Therefore all of Applicants' arguments are not found persuasive and claim 1 finally rejected (the same reference DiStefano has been applied here also).

Dependent claims 2 to 16 were alleged to be allowable for the same reasons as stated under claim1 above and because of their dependency upon allegedly allowable claim1 .

However as shown above claim 1 is not allowable. Therefore claims 2-16 are also not allowable and finally rejected.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

over

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

Feb. 28, 2006.